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(54) Storage format conversion of computer graphics

(57) An image processor converts single-band pixel components, each of which represents a single band of a multiple-band pixel, to multiple-band pixels. Data words, which include multiple single-band pixel components corresponding to first and third bands of two or more multiple-band pixels, are merged to form an interleaved data word in which respective single-band pixel components of the merged data words are interleaved. Data words, which include multiple single-band pixel components corresponding to second and fourth bands of the two or more multiple-band pixels, are merged to form a second interleaved data word in which respective single-band pixel components of the merged data words are interleaved. The first-mentioned interleaved data word and the second interleaved data word are then merged to form a third interleaved data word in which respectively single-band pixel components of the first and second interleaved data word are interleaved within one another. In one embodiment, a single read operation reads four single-band pixel components from each of three buffers which correspond to red, green, and blue bands, respectively, of a multiple-band graphical image. A single merge operation merges eight single-band pixel components representing alpha and green bands of four multiple-band pixels, and a single merge operation merges eight single-band pixel components representing blue and red bands of four multiple-band pixels. Two merge operations merge the respective merged data words to form four multiple-band pixels, each of which includes alpha, blue, green, and red components. The four multiple-band pixels are written to a destination buffer in four write operations.

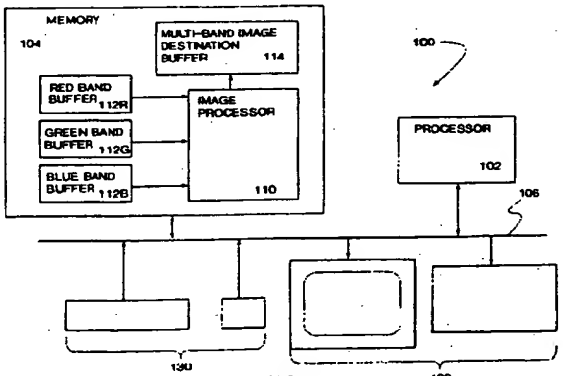

FIG. 1

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Description

FIELD OF THE INVENTION

The present invention relates to graphical image processing in a computer system and, in particular, to a particularly efficient mechanism for combining multiple separate bands of a graphical image into a single, multiple-band image buffer.

BACKGROUND OF THE INVENTION

In most computer graphics display devices in use today, color graphical images to be displayed must be in a 4-band, interleaved format in which four contiguous data components specify four respective components of a single pixel of the graphical image. For example, in some such devices, four contiguous bytes of data specify alpha, blue, green and red components, respectively, of a single pixel. It is also common to store a graphical image as multiple, separate pixel arrays for each component of which the graphical image is composed. For example, a color graphical image may be stored in the memory of a computer as three separate buffers, the first buffer including red components of the pixels of the graphical image, the second buffer including green components of the pixels of the graphical image, and the third buffer including blue components of the pixels of the graphical image.

To display a graphical image, each band of which is stored in a separate buffer, it is generally necessary to interleave the respective bands of the respective buffers into a single buffer of multiple-band pixels. For example, one such multiple-band pixel format is the general ABGR format which is generally alpha, blue, green, and red components of a single pixel stored as four respective, contiguous bytes. It is common for graphical images produced today to include approximately one million pixels. For example, common sizes for graphical images include rectangular grids of 1024-by-768 pixels or 1280-by-1024 pixels, i.e., 786,432 and 1,310,720 nixels. respectively. To produce from three separate buffers of respective bands of a graphical image a single buffer containing a four-band graphical image typically requires approximately three million read operations to read each component of each pixel from a respective one of the separate buffers and approximately four million write operations to store each band of each pixel in the single multiple-band buffer. Some conventional computer systems can store four (4) bytes in a single write operation and can therefore store approximately one million pixels in a single multiple-band buffer using approximately one million write operations. Because of the significant computer system resources required for such graphical image reformatting, a need persists in the industry for ever increasing efficiency in conversion of graphical images from multiple buffers of respective single bands of the graphical image to a single buffer of multiple bands of the graphical image.

SUMMARY OF THE INVENTION

In accordance with the present invention, respective components of two or more multiple-band pixels are read from each of two or more single-band graphical image buffers, each of which includes components of a respective band of the multiple-band pixels. Two or more components of each band are stored in respective data words. For example, (i) two or more red components of two or more respective multiple-band pixels are read from a red buffer and are stored in a red data word, (ii) two or more green components of the two or more multiple-band pixels are read from a green buffer and are stored in a green data word, and (iii) two or more blue components of the two or more multiple-band pixels are read from a blue buffer and are stored in a blue data word. Data words, which include two or more components corresponding to each of first and third bands of two or more multiple-band pixels, are merged to form an interleaved data word in which respective components of the merged data words are interleaved. For example, if the first and third bands of the multiple-band pixels are alpha and green bands, respectively, the interleaved data word includes a component representing the alpha band of a first multiple-band pixel followed by a component representing the green band of the first multiple-band pixel followed by a component representing the alpha band of a second multiple-band pixel followed by a component representing the green band of the second multiple-band pixel, and so on. Data words, which include two or more components corresponding to each of second and fourth bands of the two or more multiple-band pixels, are merged to form a second interleaved data word in which respective components of the merged data words are interleaved. For example, if the second and fourth bands of the multiple-band pixels are blue and red bands, respectively, the second interleaved data word includes components representing the following in sequence: the blue band of the first multiple-band pixel, the red band of the first multiple-band pixel, the blue band of the second multiple-band pixel, the red band of the second multiple-band pixel, and so on.

The first-mentioned interleaved data word and the second interleaved data word are then merged to form a third interleaved data word in which respective components of the first and second interleaved data words are interleaved with one another. Continuing in the above illustrative example, the third interleaved data word includes components representing the following in sequence: the alpha band of the first multiple-band pixel, the blue band of the first multiple-band pixel, the green band of the first multiple-band pixel, the red band of the first multiple-band pixel, the alpha band of the second multiple-band pixel, the blue band of the second multiple-band pixel, the green band of the second multiple-band pixel, the red band of the second multiple-

band pixel, and so on. Therefore, the third interleaved data word includes two or more multiple-band pixels in the alpha, blue, green, red format.

In one embodiment, a single read operation reads eight components from each of three buffers which correspond to red, green, and blue bands, respectively, of a multiple-band graphical image. Of the eight components of each band read using the single read operation, four components of each band are merged to form four multiple-band pixels simultaneously. A single merge operation merges eight components representing alpha and green bands of four multiple-band pixels, and a single merge operation merges eight components representing blue and red bands of the four multiple-band pixels. Two additional merge operations merge the merged data words to form four multiple-band pixels, each of which includes alpha, blue, green, and red components. Eight multiple-band pixels, each of which is four bytes in length, are written to a destination buffer in four write operations. Thus, to convert eight pixels from single-band format to multiple-band format, e.g., alpha, blue, green, and red format, requires three read operations, eight merge operations, and four write operations, i.e., a total of fifteen operations. Using prior art techniques, such format conversion of three components of each of eight pixels to eight multiple-band pixels typically requires eight read operations for each band, i.e., twenty-four read operations, and thirty-two write operations which total fifty-six operations. In addition, each component is typically moved individually into an interleaved, multiple-band format in a separate assignment operation. Thus, thirty-two assignment operations are required as well, bringing the total number of required operations to eighty-eight. As a result, the present invention represents a significant reduction of the required processing resources to convert single-band pixel components to multiple-band pixels over prior art techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system which includes an image processor which builds from separate, single-band pixel component buffers a multiple-band pixel buffer in accordance with the present invention.

Figure 2 is a logic flow diagram illustrating the construction of a multiple-band pixel buffer from separate, single-band pixel component buffers by the image processor of Figure 1 in accordance with the present invention.

Figure 3 is a block diagram illustrating merge operations used by the image processor of Figure 1 to construct from single-band pixel component buffers a multiple-band pixel buffer in accordance with the present invention.

Figure 4 is a block diagram illustrating a merge operation performed by a computer processor of Figure 1.

Figure 5 is a block diagram of the computer processor of Figure 1 in greater detail.

DETAILED DESCRIPTION

In accordance with the present invention, components of multiple-band pixels are read from multiple single-band pixel component buffers and are merged to form multiple-band pixels in an interleaved format substantially simultaneously.

Hardware Components of the Image Processing System

To facilitate appreciation of the present invention, the hardware components of the graphical image reformatting system are briefly described. Computer system 100 (Figure 1) includes a processor 102 and memory 104 which is coupled to processor 102 through a bus 106. Processor 102 fetches from memory 104 computer instructions and executes the fetched computer instructions. Processor 102 also reads data from and writes data to memory 104 and sends data and control signals through bus 106 to one or more computer display devices 120 in accordance with fetched and executed computer instructions. Processor 102 is described in greater detail below.

Memory 104 can include any type of computer memory and can include, without limitation, randomly accessible memory (RAM), read-only memory (ROM), and storage devices which include storage media such as magnetic and/or optical disks. Memory 104 includes an image processor 110, which is a computer process executing within processor 102 from memory 104. A computer process is a collection of computer instructions and data which collectively define a task performed by computer system 100. As described more completely below, image processor 110 (i) reads red, green, and blue components of pixels from buffers 112R, 112G, and 112B, respectively, (ii) combines those components to form multiple-band pixels, and (iii) stores those multiple-band pixels in destination buffer 114.

Buffers 112R, 112G, and 112B and destination buffer 114 are stored in memory 104. Buffers 112R, 112G, and 112B each store data representing individual bands of the same pixels. For example, buffers 112R, 112G, and 112B store red, green, and blue components, respectively, of the same pixels. In other words, if a particular component of data at a particular location within buffer 112R represents a red band of a particular pixel, the particular component of data at the same location within buffers 112G and 112B represent green and blue bands, respectively, of the same pixel. Therefore, buffers 112R, 112G, and 112B collectively represent a single collection of multiple-band pixels.

Destination buffer 114 can be any graphical image buffer used in graphical image processing. For example, destination buffer 114 can be a Z buffer which is used

in a conventional manner to remove hidden surfaces from a rendered graphical image. Alternatively, destination buffer 114 can be a frame buffer whose contents are immediately displayed in one of computer display devices 120. Each of computer display devices 120 can be any type of computer display device including without limitation a printer, a cathode ray tube (CRT), a light-emitting diode (LED) display, or a liquid crystal display (LCD). Each of computer display devices 120 receives from processor 102 control signals and data and, in response to such control signals, displays the received data. Computer display devices 120, and the control thereofby processor 102, are conventional.

The construction from multiple single-band buffers 112R, 112G, and 112B of multiple-band destination buffer 114 by image processor 110 is illustrated as logic flow diagram 200 (Figure 2). Processing according to logic flow diagram 200 begins with loop step 202. Loop step 202 and next step 218 define a loop in which image processor 110 (Figure 1) processes all of the components of buffers 112R, 112G, and 112G according to steps 204-216. Eight of the multiple-band pixels represented collectively by buffers 112R, 112G, and 112B are processed in a-single iteration of the loop defined by loop step 202 and next step 218. For each eight of the multiple-band pixels, processing transfers from loop step 202 to step 204.

In step 204, image processor 110 (Figure 1) reads eight components from buffer 112R in a single read operation. Processor 102 performs a read operation in which sixteen contiguous bytes of data can be read from memory 104. Image processor 110 invokes the read operation and causes processor 102 to perform a data alignment operation which shifts the read data such that the byte representing the first of the eight components of buffer 112R to be processed according to the current iteration of the loop defined by loop step 202 (Figure 2) and next 218 is aligned on an eight-byte boundary. In a preferred embodiment, image processor 110 (Figure 1) determines whether the sixteen bytes of data read in step 204 (Figure 2) are already aligned on an eight-byte boundary prior performing the data alignment operation. If the sixteen bytes of data are already so aligned, image processor 110 (Figure 1) does not perform the data alignment operation.

In this illustrative embodiment, each component of buffers 112R, 112G, and 112B which represents a band of a pixel is a single byte. While data representing eight pixels are retrieved substantially simultaneously, data representing four pixels are converted from single-band format to multiple-band format substantially simultaneously. Thus, four contiguous bytes representing respective pixel components from buffer 112R are stored in data word 312 (Figure 3) of image processor 110 (Figure 1). Data word 312 (Figure 3) includes four partitioned bytes R0-3 which represent respective ones of the first four components read from buffer 112R Image processor 110 (Figure 1) similarly includes in four partitioned bytes of a data word the second four components read from buffer 112R in a directly analogous manner. Processing transfers from step 204 (Figure 2) to step 206.

In step 206, image processor 110 (Figure 1) reads eight components from buffer 112G in a single read operation and aligns the read data and stores the first four components in data word 304 (Figure 3) of image processor 110 (Figure 1) in a manner which is directly analogous to that described above with respect to step 204. Data word 304 is directly analogous to data word 312 and includes four partitioned bytes G0-3 which correspond to, i.e., represent bands of the same pixels as the pixels whose bands are also represented by, bytes R0-3. Processing transfers from step 206 (Figure 2) to step 208.

In step 208, image processor 110 (Figure 1) reads eight components from buffer 112B in a single read operations and aligns the read data and stores the first four components in data word 310 (Figure 3) of image processor 110 (Figure 1) in a manner which is directly analogous to that described above with respect to step 204. Data word 310 is directly analogous to data words 312 and 304 and includes four partitioned bytes B0-3 which correspond to, i.e., represent bands of the same pixels as the pixels whose bands are also represented by, bytes R0-3. Processing transfers from step 208 (Figure 2) to step 210.

In this illustrative embodiment, image processor 110 (Figure 1) reads components from buffers representing red, green, and blue bands of the pixels of a graphical image and stores pixels having four bands in destination buffer 114. Therefore, image processor 110 includes a data word 302 which includes four partitioned bytes X0-3 which represent the fourth band of four respective pixels and are initialized to have values of zero. In an alternative embodiment, bytes X0-3 are read from a fourth single-band buffer in the manner described above.

In step 210 (Figure 2), image processor 110 merges bytes X0-3 and bytes G0-3 using a PMERGE operation 306 which is performed by processor 102 (Figure 1) and is illustrated in Figure 4. Data word 402 is 32-bits in length and includes four partitioned bytes 402A-D. Similarly, data word 404 is 32-bits in length and includes four partitioned bytes 404A-D. The PMERGE operation interleaves respective bytes of data words 402 and 404 into a double data word 406 as shown. Double data word 406 is 64 bits in length and includes eight partitioned bytes 406A-H. The result of PMERGE operation 306 (Figure 3) is double data word 308 which is 64-bits in length and whose eight partitioned bytes have the following values: X0, G0, X1, G1, X2, G2, X3, and G3. Image processor 110 merges the second four bytes read from buffer 112G with bytes X0-3 in a directly analogous manner. Processing transfers from step 210 (Figure 2) to step 212.

In step 212, image processor 110 (Figure 1) merges

bytes B0-3 (Figure 3) and R0-3 using a PMERGE operation 314, which is directly analogous to PMERGE operation 306 described above. The result of PMERGE operation 314 is double data word 316 which is 64-bits in length and whose eight partitioned bytes have the following values: B0, R0, B1, R1, B2, R2, B3, and R3. Image processor 110 (Figure 1) also merges the second four bytes read from buffer 112B with the second four bytes read from buffer 112R in a directly analogous manner. Processing transfers from step 212 (Figure 2) to step 214.

In step 214, image processor 110 (Figure 1) merges data words 308 (Figure 3) and 316 using PMERGE operations 318 and 322. Specifically, image processor 110 (Figure 1) merges the upper halves 308A (Figure 3) and 316A of data words 308 and 316, respectively, using PMERGE operation 318 to form double data word 320. PMERGE operation 318 is directly analogous to PMERGE operations 308 and 316 described above. Double data word 320 is a 64-bit data word which includes eight partitioned bytes whose respective values are those of bytes X0, B0, G0, R0, X1, B1, G1, and R1, respectively. Therefore, upper half 320A of double data word 320 includes bytes X0, B0, G0, and R0, which collectively represent a single four-band pixel in alpha, blue, green, and red format. Similarly, lower half 320B of double data word 320 includes bytes X1, B1, G1, and R1, which collectively represent another single four-band pixel in alpha, blue, green, and red format.

In an analogous manner, image processor 110 (Figure 1) merges lower halves 308B (Figure 3) and 316B of double data words 308 and 316, respectively, using PMERGE operation 322 to form double data word 324. PMERGE operation 322 is directly analogous to PMERGE operations 306, 314, and 318 described above. Double data word 324 is a 64-bit data word which includes eight partitioned bytes whose respective values are those of bytes X2, B2, G2, R2, X3, B3, G3, and R3, respectively. Therefore, upper half 324A of double data word 324 includes bytes X2, B2, G2, and R2, which collectively represent a third single four-band pixel in alpha, blue, green, and red format. Similarly, lower half 324B of double data word 324 includes bytes X3, B3, G3, and R3, which collectively represent a fourth single four-band pixel in alpha, blue, green, and red format.

In a manner which is directly analogous to that described above with respect to Figure 3, image processor 110 (Figure I) merges the second four bytes read from each of buffers 112B, 112G, and 112R to represent four more pixels in alpha, blue, green, and red format.

Processing transfers from step 214 (Figure 2) to step 216 in which image processor 110 (Figure 1) stores data representing the eight pixels in alpha, blue, green, and red format, including data words 320 (Figure 3) and 324, in destination buffer 114 in a single write operation. As described above, storage of pixels in destination buffer 114 can result immediately or indirectly in display of such pixels in one or more of computer display devices 120. From step 216 (Figure 2), processing transfers through next step 218 to loop step 202 in which the next eight pixels represented by buffers 112R, 112G, and 112B collectively are processed according to steps 204-216. Once all pixels represented by buffers 112R, 112G, and 112B collectively have been processed according to the loop of loop step 202 and next step 218, processing according to logic flow diagram 200 completes.

While it is generally described that all pixels represented by buffers 112R (Figure 1), 112G, and 112B collectively are processed, eight pixels per iteration of the loop of loop step 202 (Figure 2) and next step 216, some buffers do not necessarily store pixels of sequential scanlines contiguously. Therefore, in a preferred embodiment, image processor 110 (Figure 1) processes in each iteration of the loop of loop step 202 (Figure 2) and next step 218 eight pixels of a particular scanline represented by buffers 112R, 112G, and 112B collectively. In this preferred embodiment, image processor 110 (Figure 1) processes each scanline of buffers 112R, 112G, and 112B in sequence.

It is appreciated that scanlines of a particular graphical image represented by buffers 112R, 112G, and 112B sometimes has a number of pixels which is not evenly divisible by eight. In such circumstances, image processor 110 processes one, two, three, four, five, six, or seven pixels represented by buffers 112R, 112G, and 112B collectively in the manner described above with respect to steps 204-216 while ignoring excess bytes of double data words 302, 304, 310, 312, 320, and 324. For example, if scanlines of a graphical image represented by buffers 112R, 112B, and 112G include a number of pixels which is one more than an integer multiple of eight, one pixel represented by buffers 112R, 112G, and 112B is processed in the following manner for each scanline of buffers 112R, 112G, and 112B.

Image processor 110 reads one pixel from each of buffers 112R, 112G, and 112B and stores the read byte at the upper byte of each of data words 312 (Figure 3), 310, and 304, respectively, i.e., as bytes RO, GO, and B0, respectively. Data word 302 is set as described above and is not modified throughout processing according to logic flow diagram 200 (Figure 2). Bytes R1 (Figure 3), R2, R3, G1, G2, G3, B1, B2, and B3 are ignored. PMERGE operations 306, 314, 318, and 322 are executed in the manner described above. As a result, bytes X0, B0, G0, and R0 are in upper half 320A of data word 320 and are stored in destination buffer 114 (Figure 1) by image processor 110. Lower half 320B (Figure 3) of data word 320 and both halves of data word 324 are ignored.

Figure 3 also illustrates merging of components of multiple-band pixels in a multiple-band format to separate each respective band of the multiple-band pixels into separate single bands. Such is illustrated, for example, by the following example. Data word 302 includes bytes X0, X1, X2, and X3 which represent alpha,

blue, green, and red components, respectively, of a single pixel. In a directly analogous manner, respective bands of second, third, and fourth pixels are presented by respective bytes of data words 310, 304, and 312. Thus, bytes X0, B0, G0, and R0 represent alpha components of first, second, third, and fourth pixels, respectively. Similarly, (i) bytes X1, B1, G1, and R1 represent blue components of first, second, third, and fourth pixels, respectively; (ii) bytes X2, B2, G2, and R2 represent green components of first, second, third, and fourth pixels, respectively; and (iii) bytes X3, B3, G3, and R3 represent red components of first, second, third, and fourth pixels, respectively. By operation of PMERGE operations 306, 314, 318, and 322 in the manner described above, data word 320A includes alpha components of the four pixels, data word 320B includes blue components of the four pixels, data word 324A includes green components of the four pixels, and data word 324B includes red components of the four pixels.

Processor 102

Processor 102 is shown in greater detail in Figure 5 and is described briefly herein and more completely in United States patent application serial number 08/236,572 by Timothy J. Van Hook, Leslie Dean Kohn, and Robert Yung, filed April 29,1994 and entitled "A Central Processing Unit with Integrated Graphics Functions" (the '572 application) which is incorporated in its entirety herein by reference. Processor 102 includes a prefetch and dispatch unit (PDU) 46, an instruction cache 40, an integer execution unit (IEU) 30, an integer register file 36, a floating point unit (FPU) 26, a floating point register file 38, and a graphics execution unit (GRU) 28, coupled to each other as shown. Additionally, processor 102 includes two memory management units (IMMU & DMMU) & 44a-44b, and a load and store unit (LSU) 48, which in turn includes data cache 120, coupled to each other and the previously described elements as shown. Together, the components of processor 102 fetch, dispatch, execute, and save execution results of computer instructions, e.g., computer instructions of image processor 110 (Figure 1), in a pipelined manner.

PDU 46 (Figure 5) fetches instructions from memory 104 (Figure 1) and dispatches the instructions to IEU 30 (Figure 5), FPU 26, GRU 28, and LSU 48 accordingly. Prefetched instructions are stored in instruction cache 40. IEU 30, FPU 26, and GRU 28 perform integer, floating point, and graphics operations, respectively. In general, the integer operands and results are stored in integer register file 36, whereas the floating point and graphics operands and results are stored in floating point register file 38. Additionally, IEU 30 also performs a number of graphics operations, and appends address space identifiers (ASI) to addresses of load/store instructions for LSU 48, identifying the address spaces being accessed. LSU 48 generates addresses for all load and store operations. The LSU 48 also supports a number of load and store operations, specifically designed for graphics data. Memory references are made in virtual addresses. MMUs 44a-44b map virtual addresses to physical addresses.

PDU 46, IEU 30, FPU 26, integer and floating point register files 36 and 38, MMUs 44a-44b, and LSU 48 can be coupled to one another in any of number of configurations as described more completely in the '572 application. As described more completely in the '572 application with respect to Figures 8a-8d thereof, GRU 28 performs a number of distinct partitioned multiplication operations and partitioned addition operations. Various partitioned operations used by image processor 110 (Figure 1) are described more completely below.

As described above, processor 102 includes four (4) separate processing units, i.e., LSU 48, IEU 30, FPU 26, and GRU 28. Each of these processing units is described more completely in the '572 application. These processing units operate in parallel and can each execute a respective computer instruction while others of the processing units executes a different computer instruction. GRU 28 executes the merge operations described above.

In one embodiment, processor 102 is the UltraSPARC processor available from SPARC International, Inc., and computer system 100 (Figure 1) is the UltraSPARCstation available from Sun Microsystems, Inc. of Mountain View, California. Sun, Sun Microsystems, and the Sun Logo are trademarks or registered trademarks of Sun Microsystems, Inc. in the United States and other countries. All SPARC trademarks are used under license and are trademarks of SPARC International, Inc. in the United States and other countries. Products bearing SPARC trademarks are based upon an architecture developed by Sun Microsystems, Inc.

Claims

1. A method for constructing at least one multiple-band pixels from multiple single-band pixel components, the method comprising:

   (a) combining a first data word including at least two single-band pixel components representing a first band of respective multiple-band pixels with a second data word including at least two single-band pixel components representing a third band of the respective multiple-band pixels to form a first interleaved data word, which includes interleaved single-band pixel components of the first and second data words;
   (b) combining a third data word including at least two single-band pixel components representing a second band of the respective multiple-band pixels with a fourth data word including at least two single-band pixel components

representing a fourth band of the respective multiple-band pixels to form a second interleaved data word, which includes interleaved single-band pixel components of the third and fourth data words; and
(c) combining the first and second interleaved data words to form a third interleaved data word which includes at least the following single-band pixel components in the following exemplary order:

the first of the at least two single-band pixel components of the first data word;
the first of the at least two single-band pixel components of the data third word;
the first of the at least two single-band pixel components of the second data word;
the first of the at least two single-band pixel components of the fourth data word;
the second of the at least two single-band pixel components of the first data word;
the second of the at least two single-band pixel components of the third data word;
the second of the at least two single-band pixel components of the second data word; and
the second of the at least two single-band pixel components of the fourth data word.

2. The method of Claim 1 wherein steps (a) and (b) are performed by a computer processor;
further wherein each of steps (a) and (b) is performed in a single instruction cycle of the computer processor.

3. The method of Claim 1 further comprising;
reading the second, third, and fourth data words from first, second, and third buffers, respectively, which are stored in a memory of the computer.

4. The method of Claim 3 further comprising:
assigning to the first data word a predetermined value.

5. The method of Claim I further comprising:
storing the third interleaved data word in a destination buffer in a memory of the computer.

6. The method of Claim 1 wherein the first, second, third, and fourth bands of the multiple-band pixels are alpha, blue, green, and red bands, respectively.

7. A computer program product which includes a computer usable medium having computable readable code embodied therein for constructing at least one multiple-band pixels from multiple single-band pixel components, the computer readable code comprising:

(a) a first merge module configured to combine a first data word including at least two single-band pixel components representing a first band of respective multiple-band pixels with a second data word including at least two single-band pixel components representing a third band of the respective multiple-band pixels to form a first interleaved data word, which includes interleaved single-band pixel components of the first and second data words;
(b) a second merge module configured to combine a third data word including at least two single-band pixel components representing a second band of the respective multiple-band pixels with a fourth data word including at least two single-band pixel components representing a fourth band of the respective multiple-band pixels to form a second interleaved data word, which includes interleaved single-band pixel components of the third and fourth data words; and
(c) a third merge module operatively coupled to the first and second merge modules and configured to combine the first and second interleaved data words to form a third interleaved data word which includes at least the following single-band pixel components in the following exemplary order:

the first of the at least two single-band pixel components of the first data word;
the first of the at least two single-band pixel components of the third data word;
the first of the at least two single-band pixel components of the second data word;
the first of the at least two single-band pixel components of the fourth data word;
the second of the at least two single-band pixel components of the first data word;
the second of the at least two single-band pixel components of the third data word;
the second of the at least two single-band pixel components of the second data word; and
the second of the at least two single-band pixel components of the fourth data word.

8. The computer program product of Claim 7 wherein the first merge module is further configured to combine the first and second data words in a single instruction cycle of a computer processor.

9. The computer program product of Claim 7 wherein the second merge module is further configured to combine the third and fourth data words in a single instruction cycle of a computer processor.

10. The computer program product of Claim 7 further comprising:

a data reading module operatively coupled to the first and second merge modules and configured to read the second, third, and fourth data words from first, second, and third buffers, respectively, which are stored in a memory of the computer.

11. The computer program product of Claim 10 further comprising:

a first data word initialization module operatively coupled to the first merge module and configured to assign to the first data word a predetermined value.

12. The computer program product of Claim 7 further comprising:

a data writing module operatively coupled to the third merge module and configured to store the third interleaved data word in a destination buffer in a memory of the computer.

13. The computer program product of Claim 7 wherein the first, second, third, and fourth bands of the multiple-band pixels are alpha, blue, green, and red bands, respectively.

14. An image processor for constructing at least one multiple-band pixels from multiple single-band pixel components, the image processor comprising:

(a) a first merge module configured to combine a first data word including at least two single-band pixel components representing a first band of respective multiple-band pixels with a second data word including at least two single-band pixel components representing a third band of the respective multiple-band pixels to form a first interleaved data word, which includes interleaved single-band pixel components of the first and second data words;
(b) a second merge module configured to combine a third data word including at least two single-band pixel components representing a second band of the respective multiple-band pixels with a fourth data word including at least two single-band pixel components representing a fourth band of the respective multiple-band pixels to form a second interleaved data word, which includes interleaved single-band pixel components of the third and fourth data words; and
(c) a third merge module operatively coupled to the first and second merge modules and configured to combine the first and second interleaved data words to form a third interleaved data word which includes at least the following single-band pixel components in the following exemplary order:

the first of the at least two single-band pixel components of the first data word;
the first of the at least two single-band pixel components of the third data word;
the first of the at least two single-band pixel components of the second data word;
the first of the at least two single-band pixel components of the fourth data word;
the second of the at least two single-band pixel components of the first data word;
the second of the at least two single-band pixel components of the third data word;
the second of the at least two single-band pixel components of the second data word;
and the second of the at least two single-band pixel components of the fourth data word.

15. The image processor of Claim 14 wherein the first merge module is further configured to combine the first and second data words in a single instruction cycle of a computer processor.

16. The image processor of Claim 14 wherein the second merge module is further configured to combine the third and fourth data words in a single instruction cycle of a computer processor.

17. The image processor of Claim 14 further comprising:

a data reading module operatively coupled to the first and second merge modules and configured to read the second, third, and fourth data words from first, second, and third buffers, respectively, stored in a memory of the computer.

18. The image processor of Claim 17 further comprising:

a first data word initialization module operatively coupled to the first merge module and configured to assign to the first data word a predetermined value.

19. The image processor of Claim 14 further comprising:

a data writing module operatively coupled to the third merge module and configured to store the third interleaved data word in a destination buffer in a memory of the computer.

20. The image processor of Claim 14 wherein the first, second, third, and fourth bands of the multiple-band pixels are alpha, blue, green, and red bands, respectively.

21. A computer system comprising:

a memory;
a computer processor operatively coupled to the memory; and
an image processor which is stored in the memory and which includes at least one computer instructions which are executed within the computer processor to construct at least one multiple-band pixels from multiple single-band pixel components, the image processor including:

(a) a first merge module configured to combine a first data word including at least two single-band pixel components representing a first band of respective multiple-band pixels with a second data word including at least two single-band pixel components representing a third band of the respective multiple-band pixels to form a first interleaved data word, which includes interleaved single-band pixel components of the first and second data words;
(b) a second merge module configured to combine a third data word including at least two single-band pixel components representing a second band of the respective multiple-band pixels with a fourth data word including at least two single-band pixel components representing a fourth band of the respective multiple-band pixels to form a second interleaved data word, which includes interleaved single-band pixel components of the third and fourth data words; and
(c) a third merge module operatively coupled to the first and second merge modules and configured to combine the first and second interleaved data words to form a third interleaved data word which includes at least the following single-band pixel components in the following exemplary order:

the first of the at least two single-band pixel components of the first data word;
the first of the at least two single-band pixel components of the third data word;
the first of the at least two single-band pixel components of the second data word;
the first of the at least two single-band pixel components of the fourth data word;
the second of the at least two single-band pixel components of the first data word;
the second of the at least two single-band pixel components of the third data word;
the second of the at least two single-band pixel components of the second data word; and
the second of the at least two single-band pixel components of the fourth data word.

22. The computer system of Claim 21 wherein the first merge module is further configured to combine the first and second data words in a single instruction cycle of a computer processor.

23. The computer system of Claim 21 wherein the second merge module is further configured to combine the third and fourth data words in a single instruction cycle of a computer processor.

24. The computer system of Claim 21 wherein the image processor further comprises:
a data reading module operatively coupled to the first and second merge modules and configured to read the second, third, and fourth data words from first, second, and third buffers, respectively, stored in a memory of the computer.

25. The computer system of Claim 24 wherein the image processor further comprises:
a first data word initialization module operatively coupled to the first merge module and configured to assign to the first data word a predetermined value.

26. The computer system of Claim 21 wherein the image processor further comprises:
a data writing module operatively coupled to the third merge module and configured to store the third interleaved data word in a destination buffer in a memory of the computer.

27. The computer system of Claim 21 wherein the first, second, third, and fourth bands of the multiple-band pixels are alpha, blue, green, and red bands, respectively.

28. A system for distributing code (i) which is stored on a computer-readable medium, (ii) which is executable by a computer, and (iii) which includes at least one module, each of which in turn is configured to carry out at least one function to be executed by the computer, the system comprising:

(a) a first merge module configured to combine a first data word including at least two single-band pixel components representing a first band of respective multiple-band pixels with a second data word including at least two single-

band pixel components representing a third band of the respective multiple-band pixels to form a first interleaved data word, which includes interleaved single-band pixel components of the first and second data words;
(b) a second merge module configured to combine a third data word including at least two single-band pixel components representing a second band of the respective multiple-band pixels with a fourth data word including at least two single-band pixel components representing a fourth band of the respective multiple-band pixels to form a second interleaved data word, which includes interleaved single-band pixel components of the third and fourth data words; and
(c) a third merge module operatively coupled to the first and second merge modules and configured to combine the first and second interleaved data words to form a third interleaved data word which includes at least the following single-band pixel components in the following exemplary order:

the first of the at least two single-band pixel components of the first data word;
the first of the at least two single-band pixel components of the third data word;
the first of the at least two single-band pixel components of the second data word;
the first of the at least two single-band pixel components of the fourth data word;
the second of the at least two single-band pixel components of the first data word;
the second of the at least two single-band pixel components of the third data word;
the second of the at least two single-band pixel components of the second data word; and
the second of the at least two single-band pixel components of the fourth data word.

29. The system of Claim 28 wherein the first merge module is further configured to combine the first and second data words in a single instruction cycle of a computer processor.

30. The system of Claim 28 wherein the second merge module is further configured to combine the third and fourth data words in a single instruction cycle of a computer processor.

31. The system of Claim 28 further comprising:
a data reading module operatively coupled to the first and second merge modules and configured to read the second, third, and fourth data words from first, second, and third buffers, respectively, stored in a memory of the computer.

32. The system of Claim 31 further comprising:
a first data word initialization module operatively coupled to the first merge module and configured to assign to the first data word a predetermined value.

33. The system of Claim 28 further comprising:
a data writing module operatively coupled to the third merge module and configured to store the third interleaved data word in a destination buffer in a memory of the computer.

34. The system of Claim 28 wherein the first, second, third, and fourth bands of the multiple-band pixels are alpha, blue, green, and red bands, respectively.

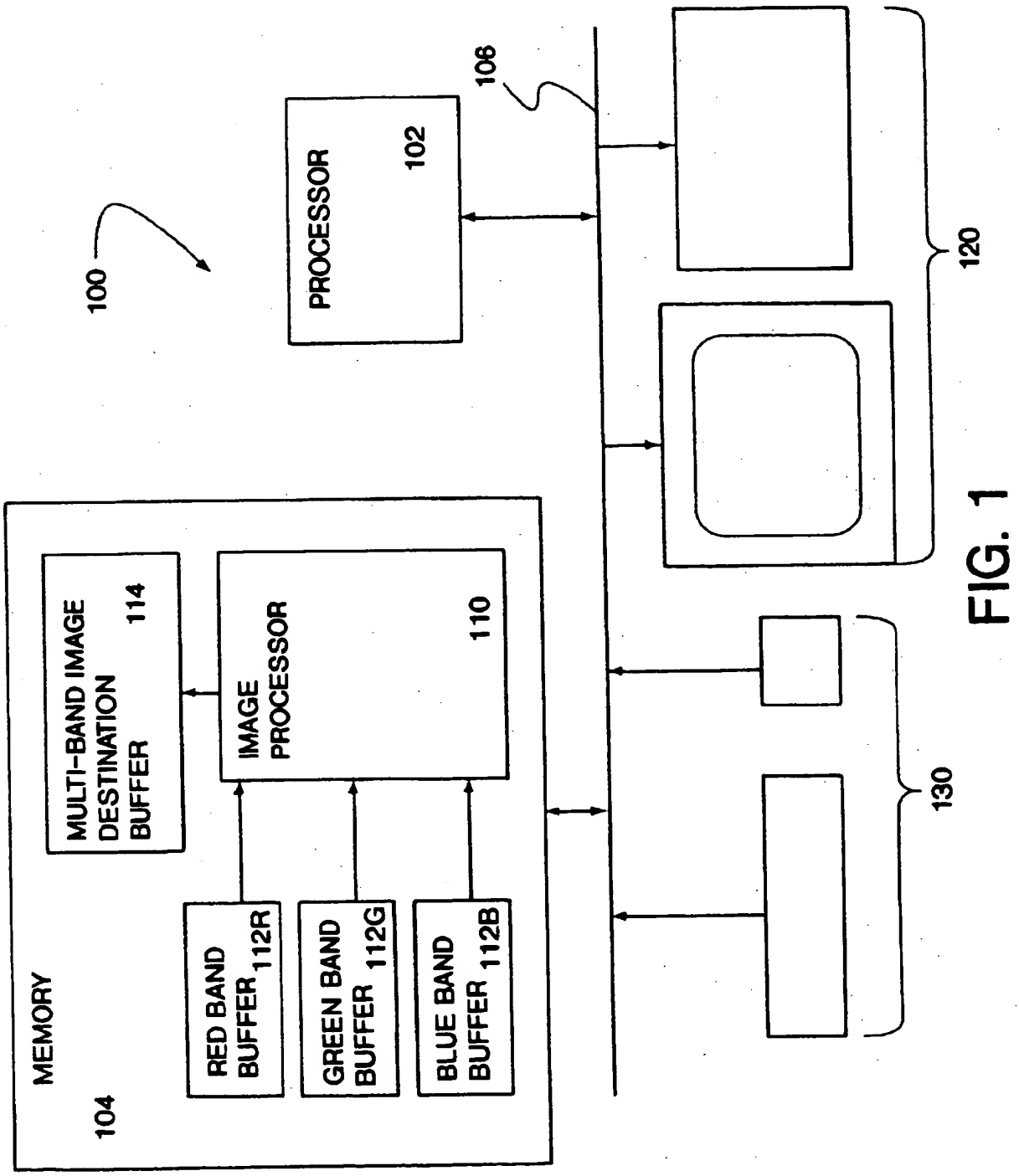


FIG. 1

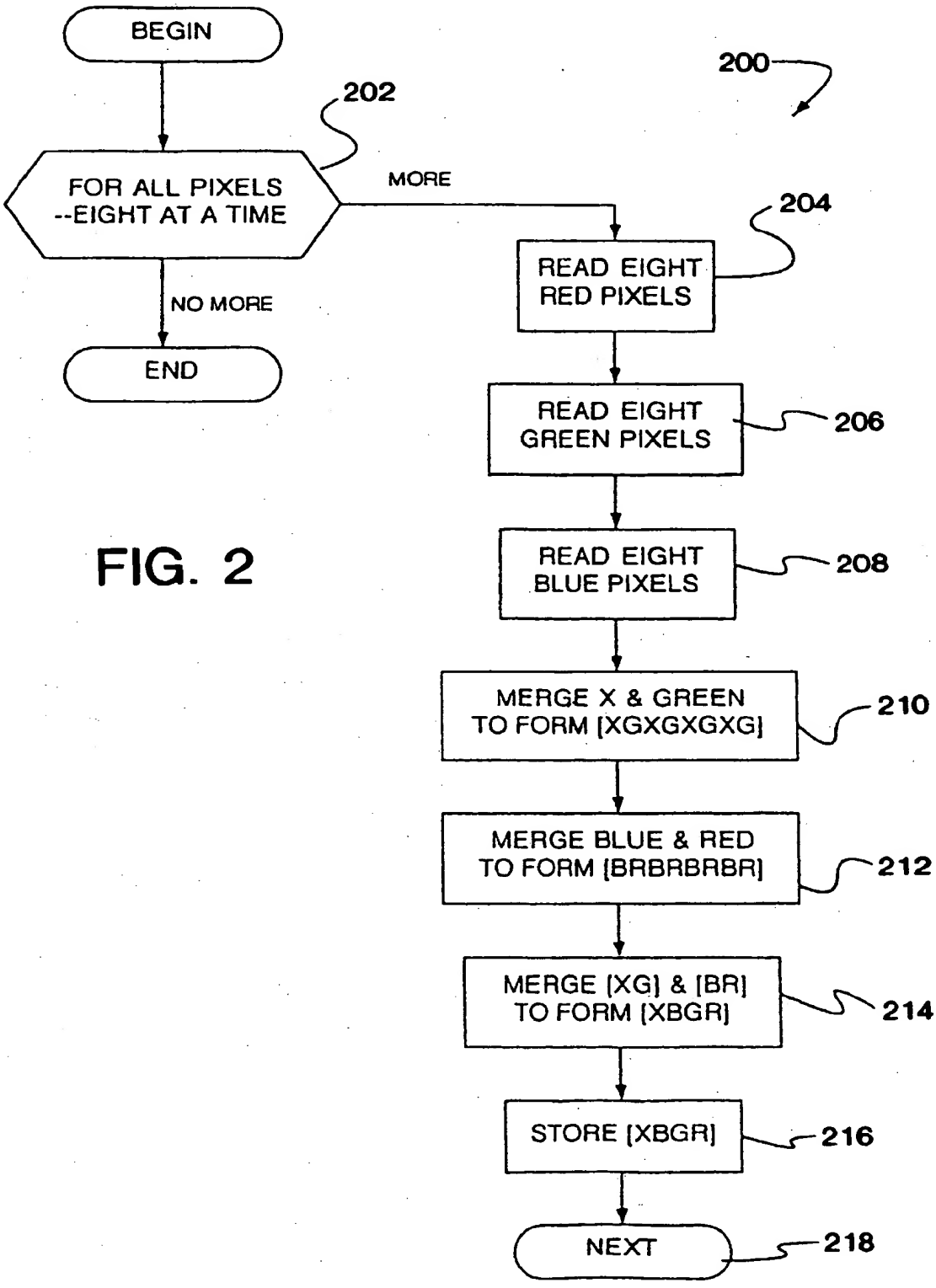
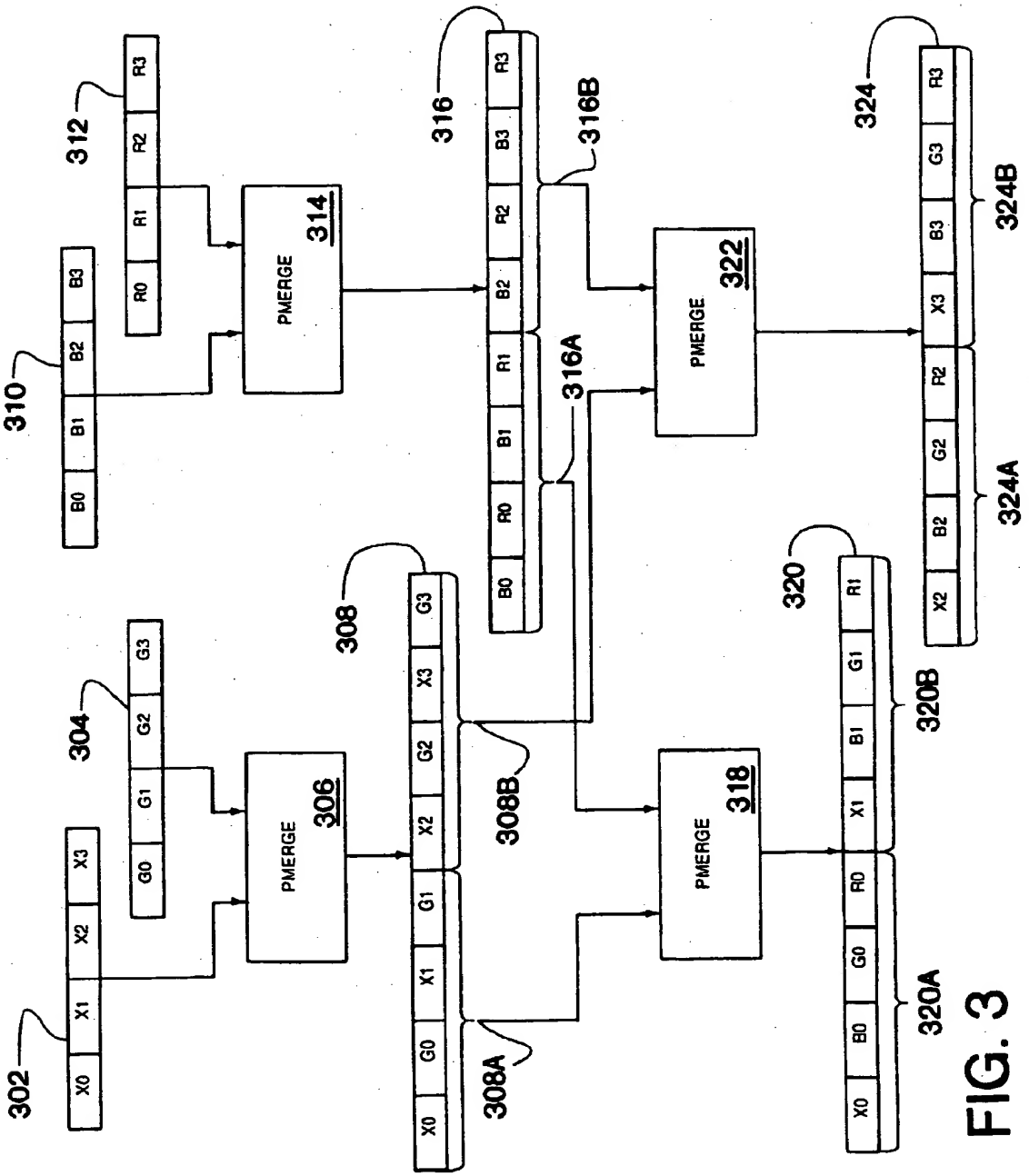


FIG. 2


302
X0
X1
X2
X3
304
G0
G1
G2
G3
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PMERGE
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308A
308B
310
B0
B1
B2
B3
312
R0
R1
R2
R3
314
316
316A
316B
318
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320A
320B
322
324
324A
324B

FIG. 3

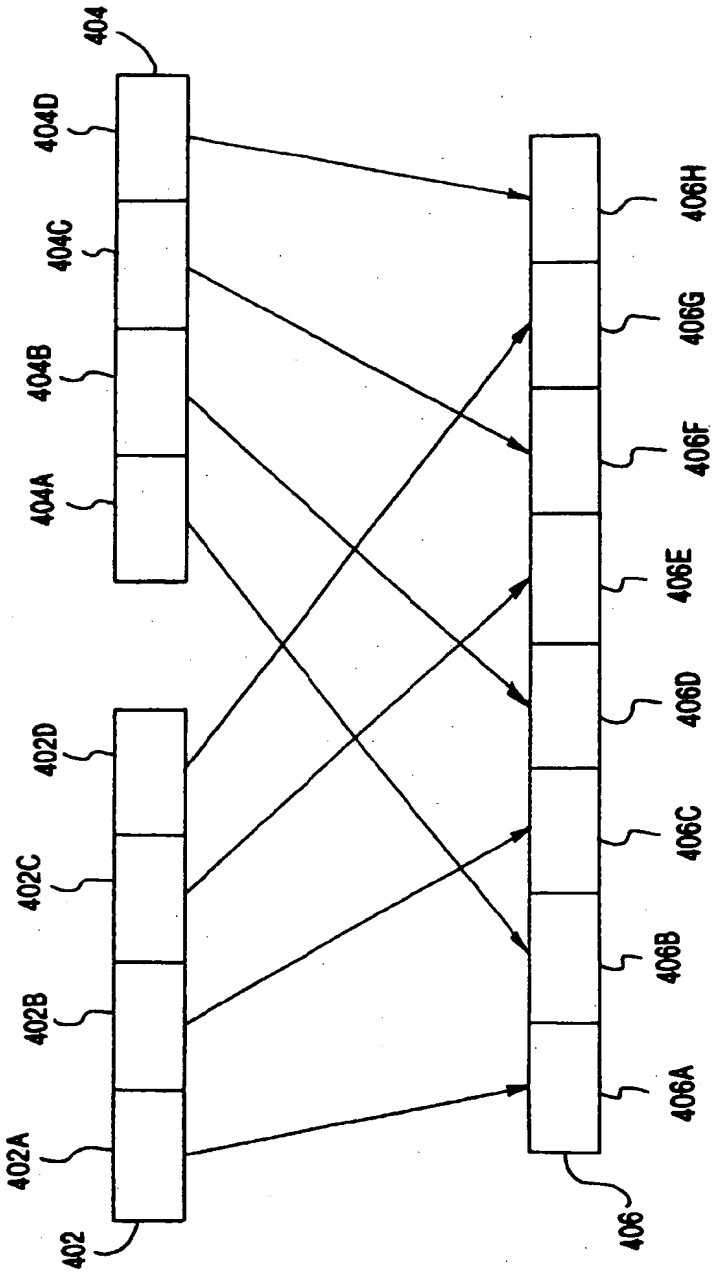
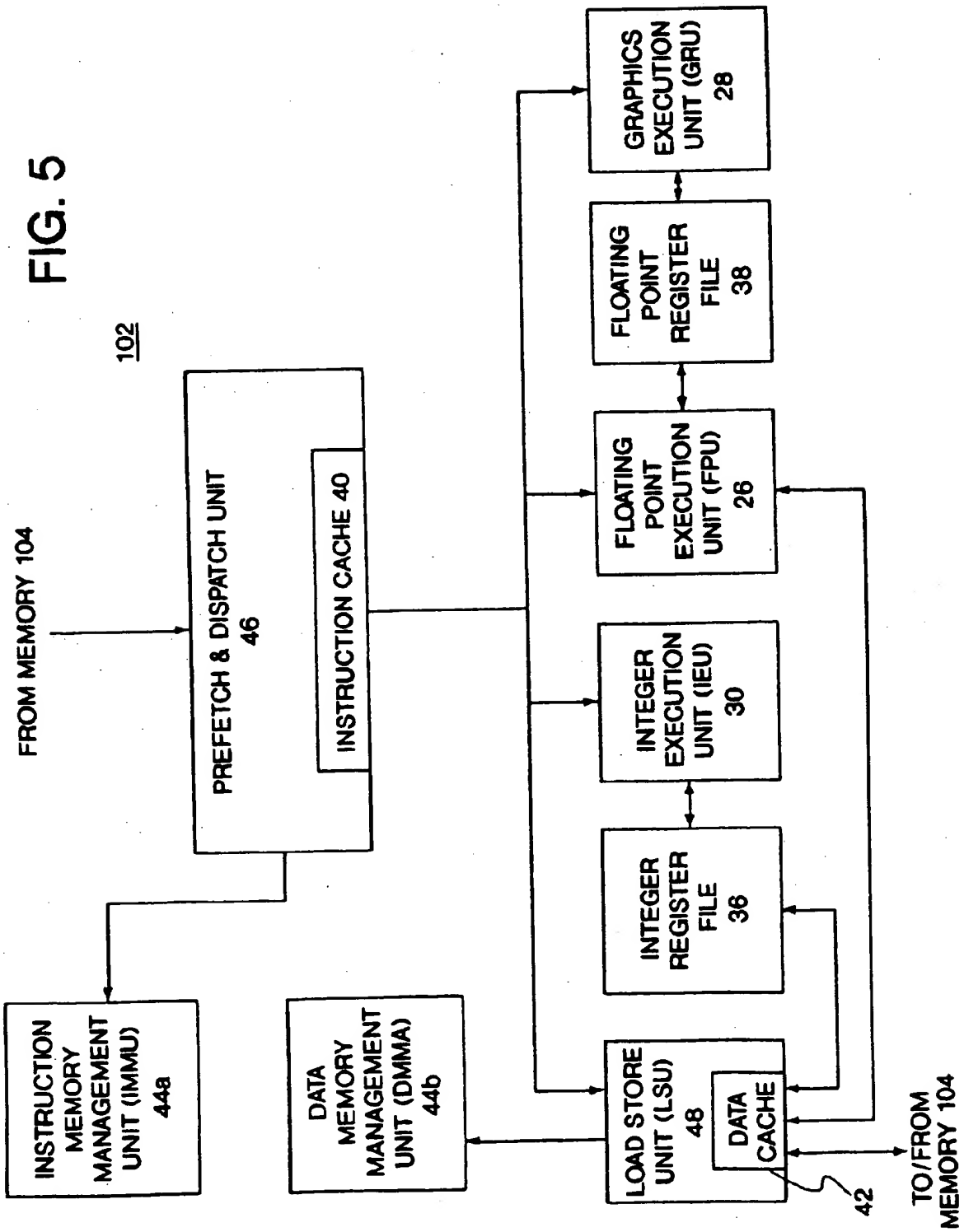


FIG. 4

FIG. 5


102
FROM MEMORY 104
PREFETCH & DISPATCH UNIT 46
INSTRUCTION CACHE 40
INSTRUCTION MEMORY MANAGEMENT UNIT (IMMU) 44a
DATA MEMORY MANAGEMENT UNIT (DMMA) 44b
LOAD STORE UNIT (LSU) 48
DATA CACHE
42
TO/FROM MEMORY 104
INTEGER REGISTER FILE 36
INTEGER EXECUTION UNIT (IEU) 30
FLOATING POINT EXECUTION UNIT (FPU) 26
FLOATING POINT REGISTER FILE 38
GRAPHICS EXECUTION UNIT (GRU) 28

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(54) Storage format conversion of computer graphics

(57) An image processor converts single-band pixel components, each of which represents a single band of a multiple-band pixel, to multiple-band pixels. Data words, which include multiple single-band pixel components corresponding to first and third bands of two or more multiple-band pixels, are merged to form an interleaved data word in which respective single-band pixel components of the merged data words are interleaved. Data words, which include multiple single-band pixel components corresponding to second and fourth bands of the two or more multiple-band pixels, are merged to form a second interleaved data word in which respective single-band pixel components of the merged data words are interleaved. The first-mentioned interleaved data word and the second interleaved data word are then merged to form a third interleaved data word in which respectively single-band pixel components of the first and second interleaved data word are interleaved within one another. In one embodiment, a single read operation reads four single-band pixel components from each of three buffers which correspond to red, green, and blue bands, respectively, of a multiple-band graphical image. A single merge operation merges eight single-band pixel components representing alpha and green bands of four multiple-band pixels, and a single merge operation merges eight single-band pixel components representing blue and red bands of four multiple-band pixels. Two merge operations merge the respective merged data words to form four multiple-band pixels, each of which includes alpha, blue, green, and red components. The four multiple-band pixels are written to a destination buffer in four write operations.

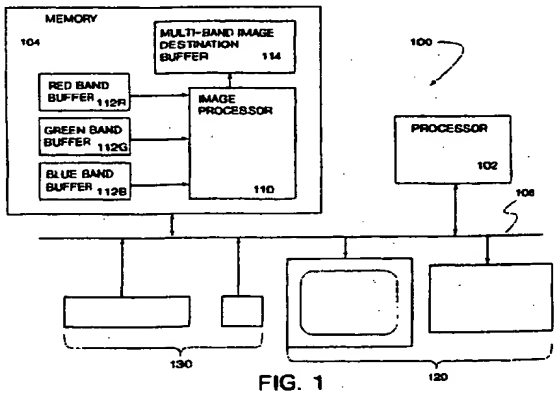

FIG. 1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 4707

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	GB 2 234 096 A (APPLE COMPUTER) * the whole document * ---	1-34	G09G1/16 G09G5/36 G06F7/00
A	WO 94 27211 A (APPLE COMPUTER) * page 11, line 1 - page 12, line 38; figures 6-8.10 * ---	1-34	
A,D	EP 0 680 013 A (SUN MICROSYSTEMS INC) * column 7, line 8 - line 35; figure 6 * -----	1-34	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G09G
G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 December 1997	Amian, D

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D : document cited in the application
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